Course title: System on Chip Design and Modelling Methods	**Neptun code: GEVAU413-a**
Course coordinator: Dr. Roland Bartók, PhD, assistant lecturer	
type of lesson and number of lessons: **lecture (2)**	
method of evaluation: colloquium	
curriculum location of the subject: (autumn/spring semester): autumn and spring	
pre-study conditions *(if any)*: Matlab Simulink; C and/or C++; Phtyon	

The task and purpose of the subject:

The course provides for PhD students advanced knowledge in system-on-a-chip modeling, simulation and design.

ARM and RISC V architectures, Soft and hard core processors for SOC, System modeling and simulation with hardware description languages, High level modeling and simulation. HIL (Hardware in the Loop) based system development.

Course description:

The course give advanced knowledge for the PhD students in embedded system hardware and software theory. Extend the knowledge of the embedded system to design methods and methodologies.

Embedded system hardware and software; Embedded system standard and user specified peripherals. Data processing units, signal conditioning with microporocessors, microcontrollers, FPGAs (Field Programmable Gate Arrays), The optimal solution for embedded systems architecture comparison for system integration, Hardware-software co-design methodologies, System development strategies, Reconfigurable computing in embedded systems, reconfiguration management, Adaptable computing technology.

Required literature:

1. René Beuchat, Florian Depraz, Andrea Guerrieri, Sahand Kashani: Fundamentals of System-on-Chip Design on Arm® Cortex®-M Microcontrollers; aRM Education Media, ISBN: 978-1-911531-35-7 (epub), pp. 659.
2. Louise H. Crockett Ross A. Elliot Martin A. Enderwitz Robert W. Stewart: Embedded Processing with the ARM® Cortex®-A9 on the Xilinx® Zynq®-7000 All Programmable SoC; Department of Electronic and Electrical Engineering University of Strathclyde Glasgow, Scotland, UK, 2017, pp. 484
3. Louise H. Crockett David Northcote Craig Ramsay Fraser D. Robinson Robert W. Stewart: Exploring Zynq® MPSoC With PYNQ and Machine Learning Applications, Department of Electronic & Electrical Engineering University of Strathclyde Glasgow, Scotland, UK. April 2019, pp. 644.

Recommended literature:

1. Ryan Kastner, Janarbek Matai, and Stephen Neuendorffer: Parallel Programming for FPGAs, http://hlsbook.ucsd.edu., 2018. pp. 235.