

Elektronikai tervezés és gyártás specializáció

Tantárgyak							
Kód.	Félév	Tárgynév	Ea.	Gy.	Köv.	Kr.	ETF
GEVAU517B	5	Digitális rendszerek komplex tervezése	2	2	V	5	GEVAU505B
GEVAU518B	5	Programozható logikák	2	2	V	5	GEVAU505B
GEVEE522B	5	Számítógépes elektronikai tervezés I.	2	2	G	5	GEVEE508B/R
GEVEE524B	5	Elektronikai technológiák	2	2	V	5	GEVEE508B/R
GEVAU519B	6	Beágyazott rendszerek	2	2	G	5	GEVAU518B
GEVEE526B	6	Komplex tervezés	0	4	G	5	GEVEE524B, GEVAU517B
GEVEE523B	6	Számítógépes elektronikai tervezés II.	2	2	G	5	GEVEE522B
GEVEE531B	6	6 hét Szakmai gyakorlat	6 hét	A	0		GEVEE524B, GEVAU517B
GEVEE521B	7	Szakdolgozat készítés	0	12	G	15	GEVEE526B, GEVEE523B, GEVEE504B
GEVEE525B	7	Tesztelés és diagnosztika	2	2	G	5	GEVEE524B

The collage illustrates the design and manufacturing process for digital electronics. It features several key components:

- Software Tools:** Screenshots of CADENCE Virtuoso (top) and Xilinx ISE (middle) showing circuit design and synthesis.
- Statistical Analysis:** A "Probability Density Graph (Runs: 1 to 30)" showing the distribution of a signal.
- Code Implementation:** A Verilog HDL code snippet for a counter:


```

      26 ---- any Xilinx primitives in this code.
      27 --library UNISIM;
      28 --use UNISIM.VComponents.all;
      29
      30 entity counter is
      31 Port ( CLOCK : in STD_LOGIC;
      32        DIRECTION : in STD_LOGIC;
      33        COUNT_OUT : out STD_LOGIC_VECTOR (3 downto 0));
      34 end counter;
      35
      36
      37 architecture Behavioral of counter is
      38 signal count_int : std_logic_vector(3 downto 0) := "0000";
      39 begin
      40 process (CLOCK)
      41 begin
      42 if CLOCK'event and CLOCK = '1' then
      43 if DIRECTION = '1' then
      44     count_int <= count_int + 1;
      45 else
      46     count_int <= count_int - 1;
      47 end if;
      48 end if;
      49 end process;
      50
      51 COUNT_OUT <= count_int;
      52 end Behavioral;
      53
      54
      
```
- PCB Design:** A detailed PCB layout showing components like U19, U18, U17, U16, U15, U14, U13, U12, U11, U10, U9, U8, U7, U6, U5, U4, U3, U2, U1, U0, and various logic components.
- Timing Diagram:** A digital timing diagram showing signals like Data_In[15:0], Clk, Reset, and various data buses over time, with a specific time point marked at 551.400 ns.
- Hardware:** Images of a Xilinx Virtex-7 XC7V2000T chip and a printed circuit board.